12. (New) The method of claim 11, wherein after the changeover operation, the test ancillary device does not store digital test data in the first digital test data until after a subsequent changeover operation.--

REMARKS

Claims 1-5 and 7-12 are pending. By this Amendment, claims 1 and 2 are amended for cosmetic purposes only, claim 6 is canceled and new claims 7-12 are added. No new matter is added. Applicants do not disclaim any equivalent of any amended limitation. Reconsideration of the above amendment and the following remarks is respectfully requested.

The Office Action rejects claims 1-6 under 35 U.S.C. §112, second paragraph, due to minor informalities. By this Amendment, claim 6 is canceled, and claims 1 and 2 are amended to obviate the informalities. As Examiner Chan has indicated that claims 1-5 contain allowable subject matter, Applicants respectfully request withdrawal of the rejection, and prompt allowance of claims 1-5.

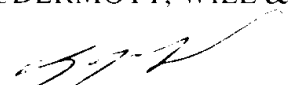
The Office Action rejects claim 6 under 35 U.S.C. §101. By this Amendment, claim 6 is canceled. Accordingly, withdrawal of the rejection of claim 6 and due consideration of new claims 7-12 are respectfully requested.

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 6 has been cancelled.

Claims 1 and 2 have been amended as follows:

1. (Amended) An apparatus for testing a semiconductor integrated circuit, comprising:

a test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test, the semiconductor integrated circuit including an analog-to-digital converter circuit for converting an analog signal to a digital signal or a digital-to-analog converter circuit for converting a digital signal to an analog signal;

a test ancillary device disposed in the vicinity of the test circuit board, [which has] the test ancillary device including data memory for storing digital test data output from the analog-to-digital converter circuit or digital test data produced by converting [the] analog test data output from the digital-to-analog converter circuit into a digital signal, and an analysis section for analyzing the digital test data stored in the data memory; wherein the data memory is divided into two memory sections such that, when digital test data [are] is stored in one memory section, [the] digital test data [that have already been] previously stored in the other memory section [are] is loaded for analysis purpose.

2. (Amended) The apparatus for testing a semiconductor integrated circuit according to claim 1, wherein the data memory has first and second memory devices, and [each of] the first and second memory devices [has] respectively include the first and second memory sections.

New claims 7-12 have been added as follows:

-- 7. (New) A method of testing a semiconductor integrated circuit, the semiconductor integrated circuit including at least one of an analog-to-digital converter circuit for converting an analog signal to a digital signal and a digital-to-analog converter circuit for converting a digital signal to an analog signal, the method using a test circuit board configured to exchange one or more signals with the semiconductor integrated circuit and a test ancillary device coupled to the test circuit board and including a memory having a first and second sections, the method comprising:

storing first digital test data derived from the semiconductor integrated circuit in the first memory section while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device configured to analyze digital test data stored in the data memory;

wherein the first and second digital test data are one of an output from the analog-to-digital converter circuit or digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal.

8. (New) The method of claim 7, wherein the semiconductor integrated circuit includes both an analog-to-digital converter circuit and digital-to-analog converter circuit, and the test ancillary device is configured to alternatively store digital test data derived from the analog-to-digital converter circuit in a first mode of operation and digital test data derived from the digital-to-analog converter circuit in a second mode of operation.

9. (New) The method of claim 7, further comprising providing a source analog signal to

the semiconductor integrated circuit, wherein the digital test data stored in the test ancillary device memory is derived from the analog-to-digital converter circuit converting the source analog signal to digital form.

10. (New) The method of claim 7, further comprising providing a source digital signal to the semiconductor integrated circuit, wherein the digital test data stored in the test ancillary device memory is derived from the digital-to-analog converter circuit converting the source digital signal to analog form.

11. (New) The method of claim 7, further comprising performing a changeover operation on the test ancillary device memory such that additional digital test data can be stored in the second memory section while the first digital test data is provided to the analysis device.

12. (New) The method of claim 11, wherein after the changeover operation, the test ancillary device does not store digital test data in the first digital test data until after a subsequent changeover operation.--